Technical Specification for Magnetic Diagnostics Data Acquisition System for SST-1

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1 Introduction

A data acquisition system is to be provided at IPR as a replacement for the existing data acquisition system for Magnetic Diagnostic application. The SST-1 (Steady State Tokamak) machine comprises of various sensors to monitor and control plasma. A number of diagnostics are involved: infra-red, soft-x-ray, imaging, magnetic etc. Magnetic diagnostics consist of probes, rogowski coil, flux loops, diamagnetic loops. The data from the magnetic diagnostics are used for control of plasma parameters such as position, shape, current etc. This document describes the system requirements of data acquisition of magnetic diagnostics and control of plasma parameters. The vendor is to provide a comprehensive, integrated solution to meet these requirements.
Below sections list the technical specifications of hardware modules along with scope of work to be carried out by the vendor.

2 Scope of Supply

2.1 Hardware Deliverables

The data acquisition and control system must be based on OpenVPX standard and suited for hard real time data acquisition and control applications. The deliverables are summarized in the table below.

Table 1

SL No.	Item Description	Qty.
1	OpenVPX system enclosure	1 No.
2	OpenVPX Single Board Computer	1 No.
3	Analog to Digital Converter modules for 96 channels	01 Set
4	Digital I/O modules, 16 DI and 16 DO	1 No.

The detailed technical specification is provided in the following sections.

2.1.1 OpenVPX system enclosure

The specifications of the required OpenVPX enclosure are stated below:

SL No.	Specification - VPX based system enclosure
1	19” Rack mount fully compliant to Eurocard, IEEE 1101.10/11
2	Advanced EMC shielded VPX system platform
3	OpenVPX compliant
4	3U Form Factor
5	Minimum 9 slots (at least 2 empty slots required, after installation of all proposed cards)
6	VPX ANSI/VITA 65 OpenVPX Compliant
7	Ambient temperature: 5°C to +50°C operation;
8	230V 50Hz AC operation
9	Power Supply ; Compatible with 3U Chassis and should Support all the proposed cards
10	Air cooled

2.1.2 OpenVPX Single Board Computer

SL No.	Specification - VPX SBC
1	Intel Xeon D processor, minimum 1.3 GHz, minimum 16 Core
2	Minimum 16 GB DDR3 memory
3	64 GB onboard NAND Flash
4	2 x Gigabit Ethernet ports
5	1 x 10 Gigabit Ethernet port
6	1 x USB 3.0 port
7	2 x USB 2.0 Ports
8	Must support at least PCIe 2 x fat pipe links
9	1 x serial port
10	2 x SATA ports
11	External SATA storage of 120 GB or higher
12	Real Time Linux Support with BSP
13	Accessories: cables and connector for connecting hard-disk and any other rear transition modules.
14	Real Time Linux Operating System with BSP for the supplied SBC

2.1.3 Analog to Digital Converter modules for 96 channels

SL No.	Specification
1	Total number of channels to be provided: 96 differential
2	Input range: ±5V (10 Vp-p) full scale
3	Sampling: Simultaneous, synchronized sampling
4	Sampling rate: Programmable upto and including 50Ks/s/channel in steps of 10KHz
5	ADC resolution: 16 bit or higher
6	Trigger: Internal and External TTL
7	Sampling Clock: Internal and External
8	Programmable sampling clock divider
9	Operation Mode: single, continuous and burst
10	Signal to Noise and Distortion ratio: 90dB minimum or better
11	THD: -80dB or better
12	Calibration; Auto calibration
13	Input impedance: ≥1MΩ
14	OpenVPX Compatible
15	Operating: 5°C to +50°C or better
16	Accessories: Rack mount Termination panels, cables for connecting ADC board to termination panel, Host bus adaptor(carrier board) if proposed card is a daughter board
17	Real time Linux device driver for the ADC module
18	Real time Linux device driver for the Host bus adaptor if proposed card is a daughter board

2.1.4 Digital I/O module 16 DI and 16 DO

SL No.	Specification
1	16 DI and 16 DO channels
2	Isolated input
3	Input and Output options: 5 V (TTL compatible)
4	Interrupt Mode for each input channels: i. Change of State ii. Edge sensitive (+ / -) iii. Level sensitive (+ / -)
5	Individual channel accessibility
6	Over voltage protection
7	OpenVPX compatible
8	Operating: 5°C to +50°C or better
9	Accessories: Rack mount Termination panels, cables for connecting DIO board to termination panel, Host bus adaptor(carrier board) if proposed card is a daughter board
10	Real time Linux device driver for the DIO module
11	Real time Linux device driver for the Host bus adaptor if proposed card is a daughter board

3 Scope of Work

3.1 Factory Acceptance Test (FAT)

Below section describes tests to be performed by the vendor on his site with each individual module in presence of IPR representative.

	Factory Acceptance Test	
	Single Board Computer (SBC) Test	**Result (P/F)**
1	Demonstrate real time operating system installation, compilation process and booting of the system	
2	Demonstrate real time operating system features for interrupt handling, task synchronization and task pre-emption (priority handling) and inter-process communication on single core and among multiple cores	
	ADC Module	
1.	Test single channel at 50 KHz in continuous mode up to 5 secs with internal clock.	
2.	Simultaneous sampling of all channels of a single board at 50 KHz in continuous mode upto 5 secs with internal clock.	
	Digital Input Output Module	
1.	Demonstrate single channel digital input access	
2.	Demonstrate single channel digital output by generating a pulse of defined duration	
3.	Demonstrate interrupt on change of state of an digital input channel	
4.	Demonstrate edge sensitive interrupt for 1 channel of digital input	
	Performance Test	
1.	Demonstrate hardware interrupt latency and jitter by using one of the	

	DIO interrupts. Interrupt latency should **be <=15 µsec** with jitter not more than **5 µsecs**.	
2.	Demonstrate **100 µsec** control loop cycle with sample control algorithm mentioned in Annexure -1 with acceptable jitter of upto **10 µsecs** for the 5 sec duration of time.	

Note:
Vendor should use real time Linux for all test programs.
Vendor should use real time Linux interrupt handler and API for demonstration of above functionalities.
The test programs and test results shall be made available to IPR.

Successful execution of FAT mentioned in above table is must and shall be acknowledged by IPR representative before dispatch of material

3.2 Site Acceptance Test (SAT)

	Single Board Computer (SBC) Test	**Result (P/F)**
1	Demonstrate real time operating system installation, compilation process and booting of the system on another hardisk to be provided by IPR during SAT	
2	Demonstrate real time operating system features for interrupt handling, task synchronization and task pre-emption (priority handling) and inter-process communication on single core and among multiple cores	
	ADC Module	
1	Simultaneous sampling of all channels of a single board at 50 KHz for different modes upto 5 secs with internal clock	
2	Simultaneous sampling of all channels (96) of all the boards at 50 KHz for 5 secs with internal clock	
3	Repeat test 1, 2 with external clock at 50 KHz	
4	Repeat test 1, 2 and 3 with external trigger	
5	Demonstrate software selectable sampling rate for all 96 channels and demonstrate different sampling rate for different boards	
6	For proving 96 channels differential +/- 5V (10V p-p) full scale, simultaneous sampling: Vendor has to give signal to all 96 channels at a same time and has to show the simultaneous sampling for all 96 channels and has to prove same from the sampled data	
7	Demonstrate the resolution in excess of or equal to14 bit using analog input from DC to full scale	
8	Signal to noise ratio 90 dB or better for all 96 channels	
	Digital Input Output Module	
1.	Demonstrate all 16 channels digital input access	
2.	Demonstrate all 16 channels digital output by generating a pulse of defined duration	
3.	Demonstrate interrupt on change of state of multiple digital input channels	
4.	Demonstrate edge sensitive interrupt for multiple digital input channels	
5	For digital input, detect minimum 1 µsec pulse signal and generate an interrupt	
6	For digital output generate minimum 1 µsec pulse	
	Integrated Test (Including ADCs, DIO and SBC)	

1	➢ Prepare ADC for 96 channels at 50 KHZ with internal clock ➢ Configure Digital input module channel for interrupt mode ➢ Start ADC acquisition from digital input pulse ➢ Demonstrate multi core functionalities for interrupt handling, data acquisition, control algorithms computation and archiving	
	Performance Test	
1	Demonstrate hardware interrupt latency and jitter by using one of the DIO interrupts. Interrupt latency should **be <=15 µsec** with jitter not more than **5µsecs**	
2	Demonstrate **100 µsecs** control loop cycle with sample control algorithm mentioned in Annexure -1 with acceptable jitter of **10 µsecs** for the 2 sec duration of time.	

Note: Vendor should use real time Linux for all test programs.

3.3 Documentation and Manual

Following shall be made available on a separate CD/DVD

1. Complete system documentation is to be supplied with User manuals, Programming Manuals, Datasheets of all the system building blocks etc.
2. Detailed documentation of kernel and real time Linux compilation and installation with sequence.
3. The FAT and SAT programs should be developed in C or C++.
4. The FAT and SAT programs and test results shall be made available to IPR

3.4 Training

The vendor has to provide end user training for a period of at least 3 working days on the configuration, operation and maintenance of the supplied system to IPR's engineers at IPR Campus.
Focus of the training is writing real time application program, compilation, debugging, performance measurement and tuning of the system.

4 Acceptance Criteria

The delivered system shall be accepted after successful completion of following

1. Inspection for visual damages and verification of the Bill of Material against mentioned specifications
2. Successful completion of FAT
3. Successful completion of SAT
4. Delivery of documentation, FAT & SAT programs and manuals
5. Completion of training

5 Warranty

The vendor has to provide minimum one year warranty for the supplied system and must provide engineering support to integrate the system with the test device, SST-1. The software support must be provided throughout the Warranty period.

6 Annexure -1

Sample control algorithm

Control loop cycle involves simultaneous 96 channels acquisition (50 KHz) with computation of 48 channels and generating output as below.

1. X_{adc}[48] ADC channels output where 48 is the number of channels to be considered.

2. Take below matrices as a constant with defined dimensionalities
    a. M[48] is a mean vector
    b. S_d[48] is a standard deviation
    c. E[48*48]
    d. G[48]
    e. C[5*48]
    f. P_{k0}[5*1]
    g. P_{kref}[5*1]
    h. D_k[4*5]

Computation:

$$X1 = \frac{X_{adc} - M}{S_d}$$

$$Y = \frac{E * X1}{G}$$

$$P_k = P_{k0} + C * Y$$

$$\Delta P_k = P_k - P_{kref}$$

$$\Delta I = D_k * \Delta P_k$$

Final output is ΔI

7 Delivery period: Within 4 (four) months from the date of purchase order.